AMENDMENTS TO THE SPECIFICATION

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please replace the paragraph starting on page 5, line 12 with the following paragraph:

Referring to FIG. 2, a block diagram of a system (or process) 200 illustrating an operation of the present invention is shown. The system 200 may be implemented to provide verification of analog signals. The system 200 may be implemented to provide connectivity verification of the analog signals. The system 200 generally comprises a source block (or state) 202 and a destination block (or state) ~~204~~ 203. The source block 202 may be configured to generate an analog signal attributed with a digital signature. The destination block ~~204~~ 203 may be configured to determine a connectivity of the attributed analog signal.

Please replace the paragraph starting on page 6, line 10 with the following paragraph:

The receive block 204 may present an analog signal to the add digital signature block 206. The add digital signature block 206 may add a digital signature to the analog signal. The digital signature may allow the system 200 to verify a connectivity of the

analog signal. The digital signature may be generated by the create digital signature block 208. The digital signature block 208 may create an unique signature for each analog signal presented to the add digital signature block 206. The attributed analog signals (e.g., the analog signals each with an added digital signature) may be presented to the destination block ~~204~~ 203.

Please replace the paragraph starting on page 6, line 20 with the following paragraph:

The destination block ~~204~~ 203 generally comprises a receive block (or state) 210, a verification decision block (or state) 212, a processing block (or state) 214 and a disable block (or state) 216. In one example, the receive block 210 may be implemented as a receive attributed signal block and the processing block 214 may be implemented as a continue processing block. However, the receive block 210 and the processing block 214 may each be implemented as another appropriate device or state in order to meet the criteria of a particular implementation.

Please replace the paragraph starting on page 7, line 8 with the following paragraph:

The receive block 210 may receive the attributed analog signal. The receive block 210 may present the attributed analog signal to the verification block 212. The verification block 212 may attempt to verify the digital signature of the analog signal. The verification block 212 may verify the digital signature to ensure proper functionality (e.g., connectivity). If the digital signature indicates proper functionality, the system 200 may continue processing of the analog signal in the block 214. If the digital signature indicates non-proper functionality, the system 200 may disable processing ~~at~~ of the analog signal at the disable block 216. The verification block 212 may determine connectivity of the analog signal being processed.

Please replace the paragraph starting on page 9, line 3 with the following paragraph:

The system 100 may provide an approach for verifying correct connectivity of analog signals within a digital simulation environment. The actual function of the analog signals cannot always be modeled within the digital simulator. However, it is generally desirable to verify the connectivity of the analog signals as early as possible in the design process. The system 100 may allow a user/designer to determine, early in the design process, connectivity of the analog signals. The system 100 may

add digital signatures on analog ports. The system ~~50~~ 100 generally adds a unique digital signature to each analog signal. The appropriate signature may be generated at a source and verified at a destination. The digital signature is generally output from an analog source and input to an analog destination. Such an implementation may allow the connectivity of the analog signals to be verified within a digital simulator.

Please replace the paragraph starting on page 10, line 20 with the following paragraph:

The system 100 may be implemented to verify the connectivity and correctness of analog circuitry within a complex logic design. The system 100 may create ~~an~~ a unique digital signature for each unique analog source and add code to a model of an analog block to cause the unique signature to be generated within a digital simulator. The added code may be implemented to allow the digital simulator to detect and verify the unique digital signature. The system 100 may allow a digital simulator to verify a correct connectivity of an analog signal within a digital simulator. The system 100 may allow a digital simulator to verify that a number of analog signals have been correctly connected.